

# HITACHI

Hitachi Displays, Ltd.

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## TECHNICAL DATA TX70D12VC0CAB

### CONTENTS

No.	Item	Sheet No.	Page
-	COVER	3284PS2601 - TX70D12VC0CAB - 1	1-1/1
-	RECORD OF REVISION	3284PS2602 - TX70D12VC0CAB - 1	2-1/1
-	DESCRIPTION	3284PS2603 - TX70D12VC0CAB - 1	3-1/1
1	ABSOLUTE MAXIMUM RATINGS	3284PS2604 - TX70D12VC0CAB - 1	4-1/1
2	OPTICAL CHARACTERISTICS	3284PS2605 - TX70D12VC0CAB - 1	5-1/2 - 2/2
3	ELECTRICAL CHARACTERISTICS	3284PS2606 - TX70D12VC0CAB - 1	6-1/1
4	BLOCK DIAGRAM	3284PS2607 - TX70D12VC0CAB - 1	7-1/1
5	INTERFACE PIN ASSIGNMENT	3284PS2608 - TX70D12VC0CAB - 1	8-1/5 - 5/5
6	INTERFACE TIMING	3284PS2609 - TX70D12VC0CAB - 1	9-1/3 - 3/3
7	DIMENSIONAL OUTLINE	3284PS2610 - TX70D12VC0CAB - 1	10-1/2 - 2/2
8	DESIGNATION LOT MARK	3284PS2611 - TX70D12VC0CAB - 1	11-1/1
9	COSMETIC SPECIFICATIONS	3284PS2612 - TX70D12VC0CAB - 1	12-1/3 - 3/3
10	PRECAUTION	3284PS2613 - TX70D12VC0CAB - 1	13-1/3 - 3/3

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## DESCRIPTION

The following specifications are applied to the following Super-TFT module.

Note : Inverter for back light unit is not built in this module.

**Product Name : TX70D12VC0CAB**

### General Specifications

Effective Display Area	: (H)599.04×(V)359.42	(mm)
Number of Pixels	: (H)1,280×(V)768	(pixels)
Pixel Pitch	: (H)0.468×(V)0.468	(mm)
Color Pixel Arrangement	: R+G+B Vertical Stripe	
Display Mode	: Transmissive Mode Normally Black Mode	
Top Polarizer Type	: Anti Glare	
Number of Colors	: 16,777,216	(colors)
Viewing Angle Range	: Super Wide Version (Horizontal & Vertical : 176°, CR≥10)	
Input Signal	: 1-channel LVDS (LVDS:Low Voltage Differential Signaling)	
Back Light	: 14 pcs. of CCFL	
External Dimensions	: (H)678.0×(V)414.0×(t)37.0	(mm)
Weight	: 6,500g typ.	

## 1. ABSOLUTE MAXIMUM RATINGS

### 1.1 Environmental Absolute Maximum Ratings

ITEM	Operating		Storage		Unit	Note
	Min.	Max.	Min.	Max.		
Temperature	0	50	-20	60	°C	1), 5)
Humidity	2)		2)		%RH	1)
Vibration	-	4.9(0.5G)	-	9.8 (1G)	m/s <sup>2</sup>	3)
Shock	-	29.4(3G)	-	294 (30G)	m/s <sup>2</sup>	4)
Corrosive Gas	Not Acceptable		Not Acceptable		-	
Illumination at LCD Surface	-	50,000	-	50,000	lx	

Note 1) Temperature and Humidity should be applied to the glass surface of a Super-TFT module, not to the system installed with a module.

The temperature at the center of rear surface should be less than 60°C on the condition of operating. The brightness of a CCFL tends to drop at low temperature. Besides, the life-time becomes shorter at low temperature.

2)  $T_a \leq 40^\circ\text{C}$  ..... Relative humidity should be less than 85%RH max. Dew is prohibited.

$T_a > 40^\circ\text{C}$  ..... Relative humidity should be lower than the moisture of the 85%RH at 40°C.

3) Frequency of the vibration is between 15Hz and 100Hz. (Remove the resonance point)

4) Pulse width of the shock is 10 ms.

5) Long operation under low temperature may cause some portion of display area to be reddish for several minutes after turning on the product.

However, it does not affect the characteristics and reliability of the product.

### 1.2 Electrical Absolute Maximum Ratings

#### (1) Super-TFT Module

$V_{SS} = 0\text{ V}$

ITEM	SYMBOL	Min.	Max.	Unit	Note
Power Supply Voltage	$V_{DD}$	0	13.2	V	
Input Voltage for logic	$V_I$	-0.3	3.6	V	1)
Electrostatic Durability	$V_{ESD0}$	$\pm 100$		V	2),3)
	$V_{ESD1}$	$\pm 8$		k V	2),4)

Note 1) It is applied to pixel data signal and clock signal.

2) Discharge Coefficient : 200pF-250  $\Omega$ , Environmental : 25°C-70%RH

3) It is applied to I/F connector pins.

4) It is applied to the surface of a metallic bezel and a LCD panel.

#### (2) Back-light

$GND = 0\text{ V}$

ITEM	SYMBOL	Min.	Max.	Unit	Note
Input Current	$I_L$	-	7.0	mA <sub>rms</sub>	1)
Input Voltage	$V_L$	-	1800	V <sub>rms</sub>	2)

Note 1) The specification shall be applied to each CFL. The specification is defined at ground line.

2) The specification shall be applied at connector pins for a CFL at start-up.

## 2. OPTICAL CHARACTERISTICS

The following optical characteristics are measured under stable conditions. It takes about 30 minutes to reach stable conditions. The measuring point is the center of display area unless otherwise noted.

The optical characteristics should be measured in a dark room or equivalent state.

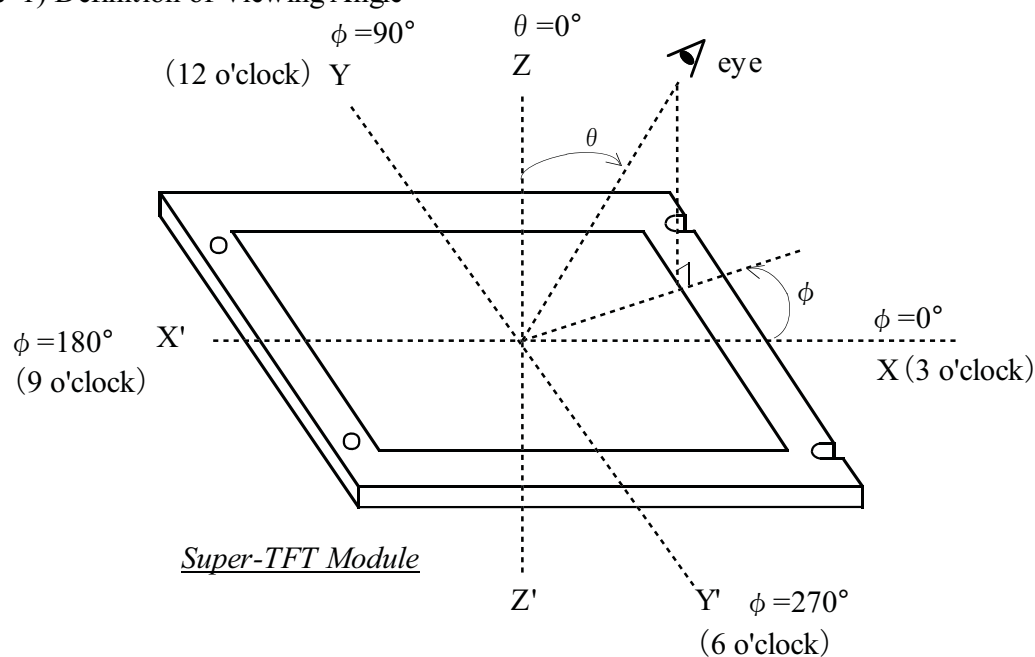
Measuring equipment : Pritchard 1980A, or equivalent

Temperature = 25°C、VDD = 12.0V、f V = 60Hz、

IL = 5.0mA (average of 14 pieces of CFLs, PWM:Duty 100%) , CTL = Low

ITEM		SYMBOL	CONDITION	Min.	Typ.	Max.	UNIT	NOTE
Contrast Ratio		CR	$\theta = 0^\circ$ 1)	350	500	-	-	2)
Response Time	Rise	ton		-	13	30	ms	3), CTL:High
	Fall	toff		-	13	30	ms	3), CTL:High
Brightness of white		Bwh		350	470	-	cd/m <sup>2</sup>	
Brightness uniformity		Buni		-	-	30	%	4)
Color Chromaticity (CIE)	Red	$\chi$		0.61	0.64	0.67	-	[Gray scale =255]
		y		0.29	0.32	0.35		
	Green	$\chi$		0.26	0.29	0.32		
		y		0.58	0.61	0.64		
	Blue	$\chi$		0.12	0.15	0.18		
		y		0.04	0.07	0.10		
	White	$\chi$		0.245	0.275	0.305		
		y		0.252	0.282	0.312		
Variation of Color Position (CIE)	Red	$\Delta \chi$	$\theta = +50^\circ$ $\phi = 0^\circ, 90^\circ$ $180^\circ, 270^\circ$ 1)	-	-	0.04	-	5) [Gray scale =255]
		$\Delta y$		-	-	0.04		
	Green	$\Delta \chi$		-	-	0.04		
		$\Delta y$		-	-	0.04		
	Blue	$\Delta \chi$		-	-	0.04		
		$\Delta y$		-	-	0.04		
	White	$\Delta \chi$		-	-	0.04		
		$\Delta y$		-	-	0.04		
Contrast Ratio at 88°		CR88°	10	-	-	-	Estimated value.	

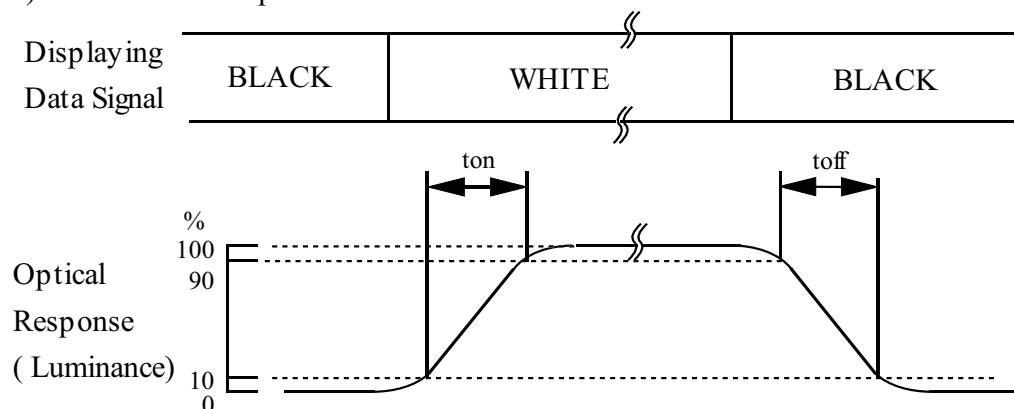
## Note 1) Definition of Viewing Angle



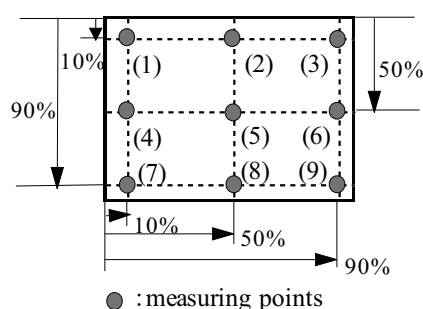
## 2) Definition of Contrast Ratio (CR)

$$CR = \frac{\text{(Luminance at displaying WHITE)}}{\text{(Luminance at displaying BLACK)}}$$

## 3) Definition of Response Time



## 4) Definition of Brightness Uniformity



Display pattern is white (255 level). The brightness uniformity is defined as the following equation. Brightness at each point is measured, and average, maximum and minimum brightness is calculated.

$$B_{uni} = \frac{|B_{max \text{ or } B_{min}} - B_{ave}|}{B_{ave}} \times 100$$

where,  $B_{max}$  = Maximum brightness

$B_{min}$  = Minimum brightness

$$B_{ave} = \text{Average brightness} = \frac{\sum_{k=1}^9 (B(k))}{9}$$

5) Variation of color position on CIE is defined as difference between colors at  $\theta = 0^\circ$  and at  $\theta = 50^\circ$  &  $\phi = 0^\circ, 90^\circ, 180^\circ, 270^\circ$ .

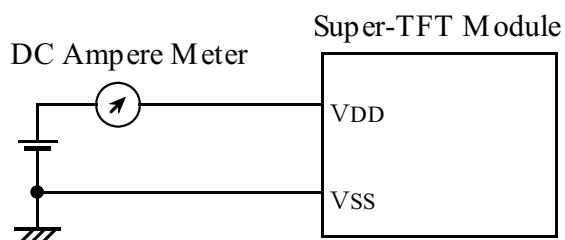
### 3. ELECTRICAL CHARACTERISTICS

#### 3.1 TFT-LCD Module

Ta=25°C, Vss=0V

ITEM	SYMBOL	Min.	Typ.	Max.	Unit	Note
Power Supply Voltage	VDD	11.4	12.0	12.6	v	
Power Supply Current	IDD	—	0.57	0.80	A	1),2)
Ripple Voltage of Power Supply	VDDR	—	—	0.15	V	

Note 1) DC current at fv=60.0Hz, fCLK=82MHz, VDD=12.0V and white pattern.



- 2) Current fuse is built in a module. Current capacity of power supply for VDD should be larger than 4A, so that the fuse can be opened at the trouble of power supply.

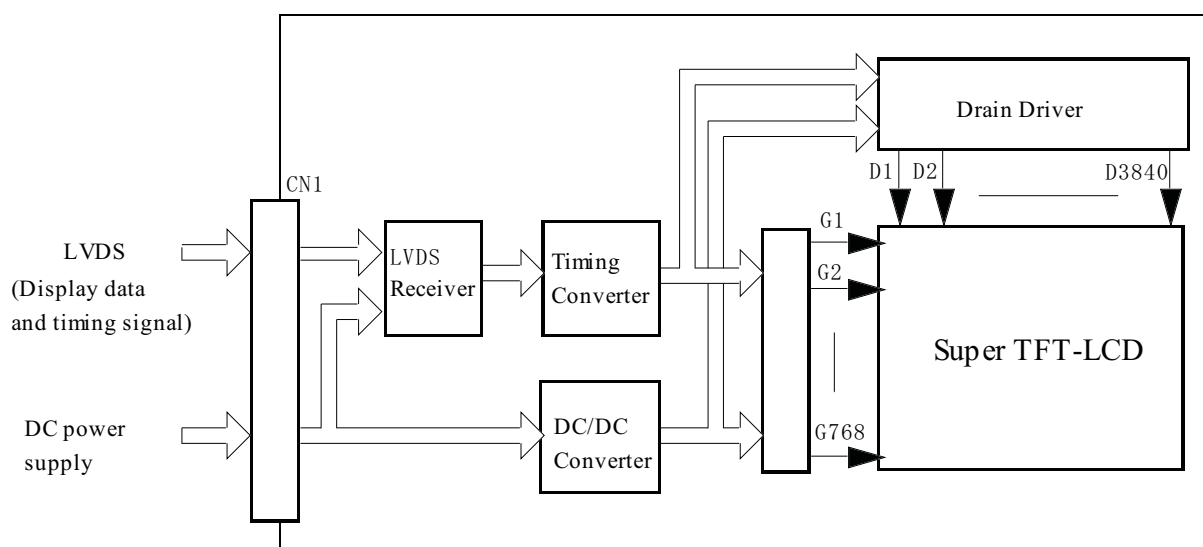
#### 3.2 Back Light

ITEM	SYMBOL	Min.	Typ.	Max.	Unit	Note
Input Current	IL	3.0	5.0	6.0	mArms	1)
Input Voltage	VL	-	1140	-	Vrms	
Frequency	f0	50	55	60	kHz	2)
Kick-Off Voltage	Vs	-	-	1600	V	3)
CFL Life Time		60,000	-	-	hours	4)

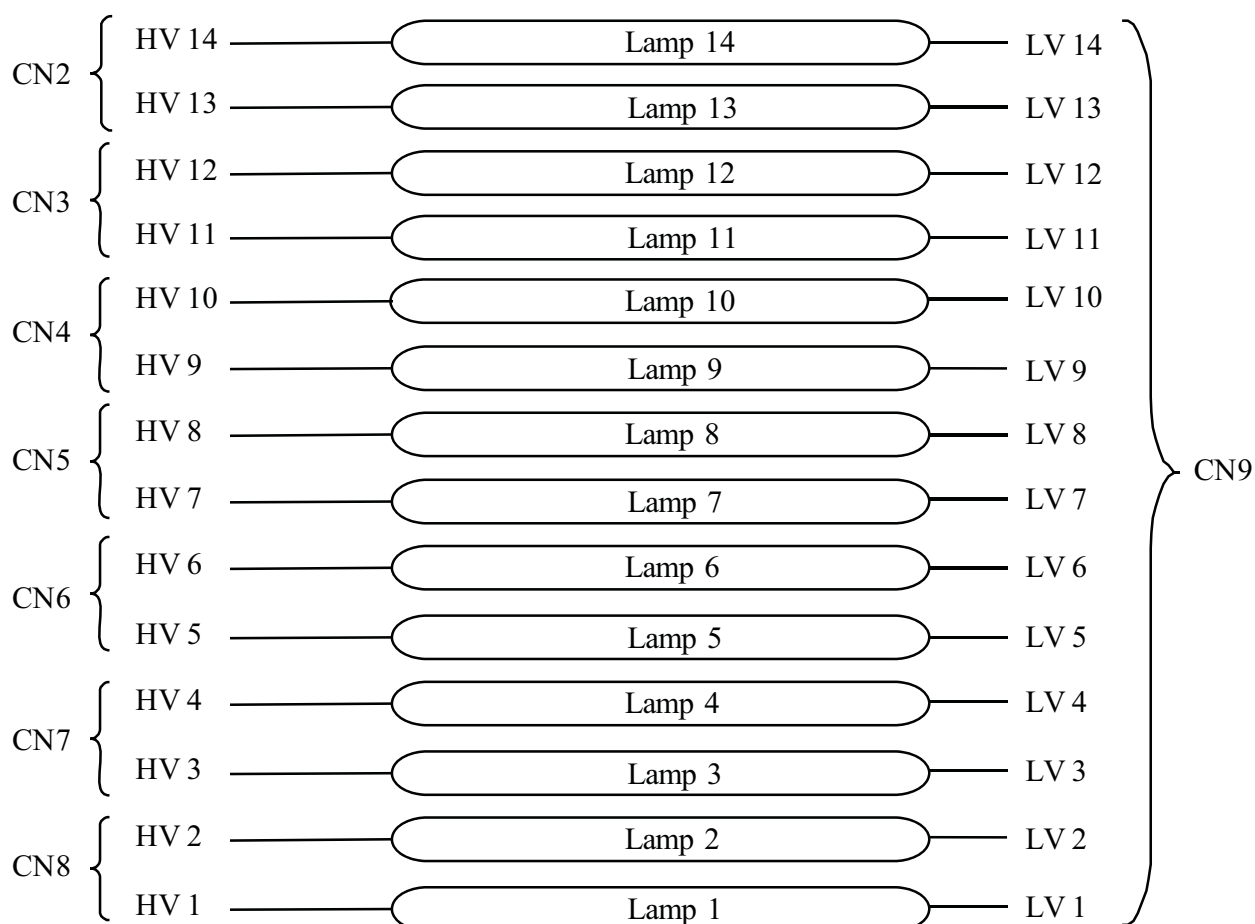
- Notes
- 1) The specification shall be applied to each CFL. The specification is defined at ground line.
  - 2) Frequency of power supply for a CFL may cause the interference with HSYNC frequency and cause beat or flicker on the display. Therefore, lamp frequency shall be as different as possible from HSYNC frequency in order to avoid the interference.
  - 3) Ta = 0 degree
  - 4) Life time of a lamp is defined. The life is determined as the time at which brightness of the lamp is 50% compared to that of initial value at the typical lamp current on condition of continuous operation at  $25 \pm 2^\circ\text{C}$ . IL=4.0mA (Duty 100%)

## 4. BLOCK DIAGRAM

### (1) Super-TFT Module



### (2) Back light unit





## 5. INTERFACE PIN ASSIGNMENT

### 5.1 TFT-LCD MODULE

CN1 : JAE FI-SEB20P-HF13

(Matching connector : JAE FI-SE20M or equivalent)

Pin No.	Symbol	Description	Note
1	VDD	Power Supply (typ.+12V)	1)
2	VDD		
3	VSS	GND (0V)	2)
4	VSS		
5	Rx0-	Pixel Data	3)
6	Rx0+		
7	VSS	GND (0V)	2)
8	Rx1-	Pixel Data	3)
9	Rx1+		
10	VSS	GND (0V)	2)
11	Rx2-	Pixel Data	3)
12	Rx2+		
13	VSS	GND (0V)	2)
14	CLK-	Pixel Clock	3)
15	CLK+		
16	VSS	GND (0V)	2)
17	Rx3-	Pixel Data	3)
18	Rx3+		
19	VSS	GND (0V)	2)
20	CTL	Low:A line trace ON, High:A line trace OFF	4)

- Notes
- 1) All VDD pins shall be connected to +12.0V(Typ.).
  - 2) All VSS pins shall be grounded. Metal bezel is internally connected to VSS.
  - 3) Rx n+ and Rx n- (n=1,2,3) should be wired by twist-pairs or side-by-side FPC patterns, respectively.
  - 4) Low level : 0~0.15V , High level : 2.5~5.0V

### 5.2 BACK-LIGHT UNIT

CN2,CN3,CN4,CN5,CN6,CN7,CN8 : JST BHR-03VS-1

(Matching connector : JST SM02 (8.0) B-BHS-1-TB or equivalent)

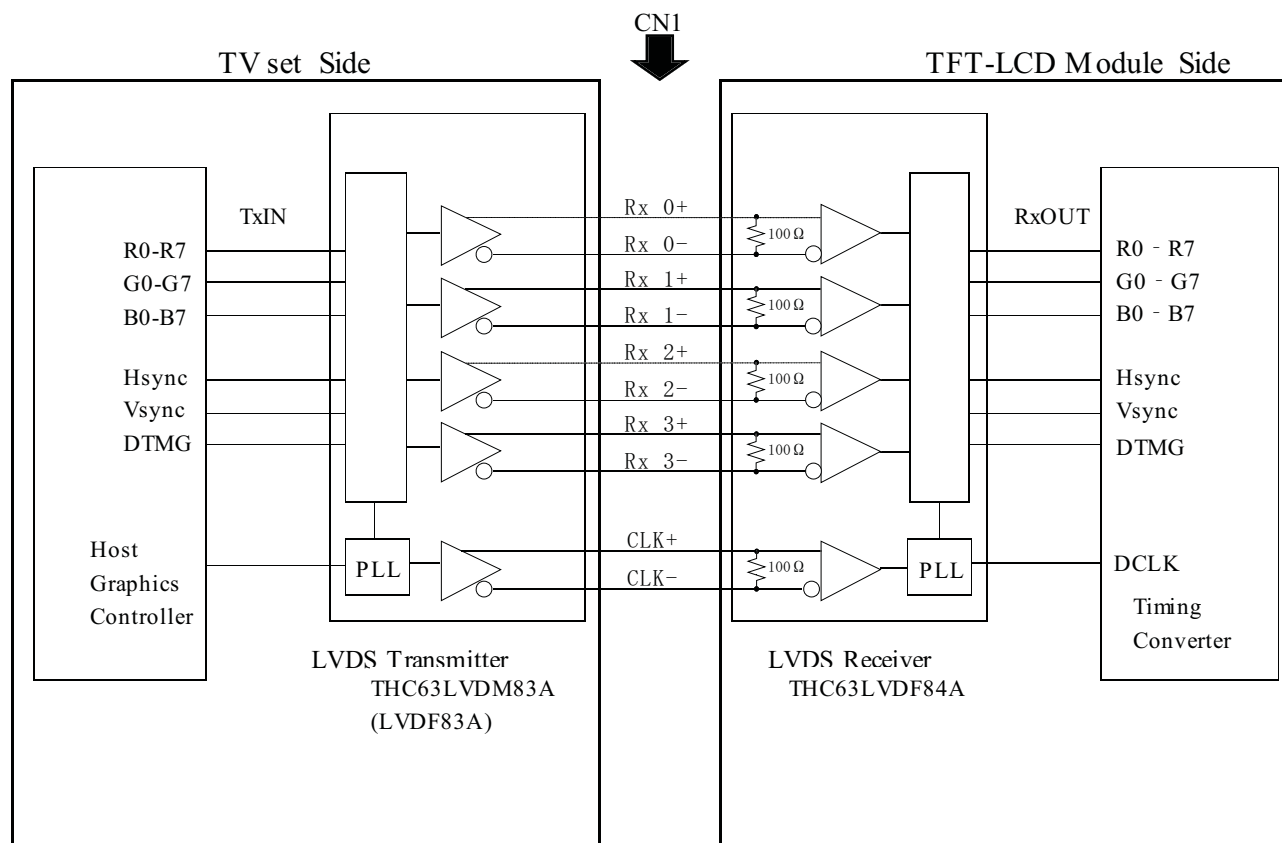
Pin No.	SYMBOL	Function
1	VL	Power Supply for Lamp Even side (High Voltage)
2	NC	
3	VL	Power Supply for Lamp Odd side (High Voltage)

CN9 : JST PHR14

(Matching connector : JST S14B-PH-SM3-TB or equivalent)

Pin No.	SYMBOL	Function
1	LV 1	Lamp 1 LV
2	LV 2	Lamp 2 LV
3	LV 3	Lamp 3 LV
4	LV 4	Lamp 4 LV
5	LV 5	Lamp 5 LV
6	LV 6	Lamp 6 LV
7	LV 7	Lamp 7 LV
8	LV 8	Lamp 8 LV
9	LV 9	Lamp 9 LV
10	LV 10	Lamp 10 LV
11	LV 11	Lamp 11 LV
12	LV 12	Lamp 12 LV
13	LV 13	Lamp 13 LV
14	LV 14	Lamp 14 LV

## BLOCK DIAGRAM OF INTERFACE



R0~R7 : Pixel R Data  
 G0~G7 : Pixel G Data  
 B0~B7 : Pixel B Data  
 HSYNC : Horizontal synchronization signal  
 VSYNC : Vertical synchronization signal  
 DTMG : Display timing signal

- Notes
- 1) The system must have the transmitter to drive the module.
  - 2) LVDS cable impedance shall be 50 ohms per signal line or about 100 ohms per twist-pair line when it is used differentially.

**LVDS INTERFACE**

	SIGNAL	TRANSMITTER THC63LVDM83A		INTERFACE CONNECTOR		RECEIVER THC63LVDF84A		TFT CONTROL INPUT
		PIN	INPUT	PC	TFT-LCD	PIN	OUTPUT	
24bit	R2	51	Tx IN0	TA OUT0+	Rx 0+	27	Rx OUT0	R2
	R3	52	Tx IN1			29	Rx OUT1	R3
	R4	54	Tx IN2			30	Rx OUT2	R4
	R5	55	Tx IN3			32	Rx OUT3	R5
	R6	56	Tx IN4	TA OUT0-	Rx 0-	33	Rx OUT4	R6
	R7	3	Tx IN6			35	Rx OUT6	R7
	G2	4	Tx IN7			37	Rx OUT7	G2
	G3	6	Tx IN8			38	Rx OUT8	G3
	G4	7	Tx IN9	TA OUT1+	Rx 1+	39	Rx OUT9	G4
	G5	11	Tx IN12			43	Rx OUT12	G5
	G6	12	Tx IN13			45	Rx OUT13	G6
	G7	14	Tx IN14			46	Rx OUT14	G7
	B2	15	Tx IN15	TA OUT1-	Rx 1-	47	Rx OUT15	B2
	B3	19	Tx IN18			51	Rx OUT18	B3
	B4	20	Tx IN19			53	Rx OUT19	B4
	B5	22	Tx IN20			54	Rx OUT20	B5
	B6	23	Tx IN21	TA OUT2+	Rx 2+	55	Rx OUT21	B6
	B7	24	Tx IN22			1	Rx OUT22	B7
	HSYNC	27	Tx IN24			3	Rx OUT24	HSYNC
	VSYNC	28	Tx IN25			5	Rx OUT25	VSYNC
	DTMG	30	Tx IN26	TA OUT2-	Rx 2-	6	Rx OUT26	DTMG
	R0	50	Tx IN27			7	Rx OUT27	R0
	R1	2	Tx IN5			34	Rx OUT5	R1
	G0	8	Tx IN10			41	Rx OUT10	G0
	G1	10	Tx IN11	TA OUT3+	Rx 3+	42	Rx OUT11	G1
	B0	16	Tx IN16			49	Rx OUT16	B0
	B1	18	Tx IN17			50	Rx OUT17	B1
	RSVD 1)	25	Tx IN23			2	Rx OUT23	not connect
	DCLK	31	TxCLK IN	TxCLK OUT+ TxCLK OUT-	RxCLK IN+ RxCLK IN-	26	RxCLK OUT	DCLK

R0~R7 : Pixel R Data (7 ; MSB, 0 ; LSB)

G0~G7 : Pixel G Data (7 ; MSB, 0 ; LSB)

B0~B7 : Pixel B Data (7 ; MSB, 0 ; LSB)

HSYNC : Horizontal synchronization signal

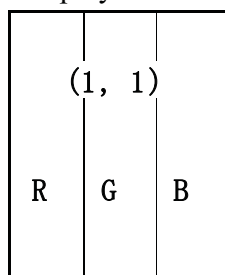
VSYNC : Vertical synchronization signal

DTMG : Display timing signal

Notes 1) RSVD(reserved) pins on the transmitter shall be "H" or "L".

## CORRESPONDENCE BETWEEN INPUT DATA AND DISPLAY IMAGE

Display data of adjacent one pixel is latched during one cycle of DCLK.

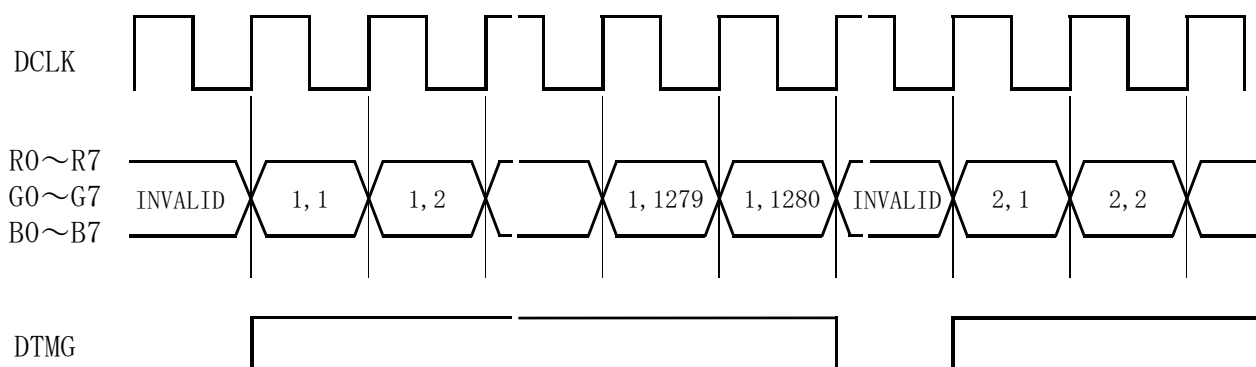


pixel : R0~R7 :R data

G0~G7 :G data

B0~B7 :B data

1, 1	1, 2	1, 3	_____	1, 1280
2, 1	2, 2	2, 3	_____	2, 1280
3, 1	3, 2	3, 3	_____	3, 1280
⋮	⋮	⋮		⋮
768, 1	768, 2	768, 3	_____	768, 1280



**RELATIONSHIP BETWEEN DISPLAY COLORS AND INPUT SIGNALS**

Color		Red Data								Green Data								Blue Data							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
		MSB								LSB								MSB							
Basic Color	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue (255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (2)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
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	Red (254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Green	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Green(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
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	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green(254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Blue	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue(254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

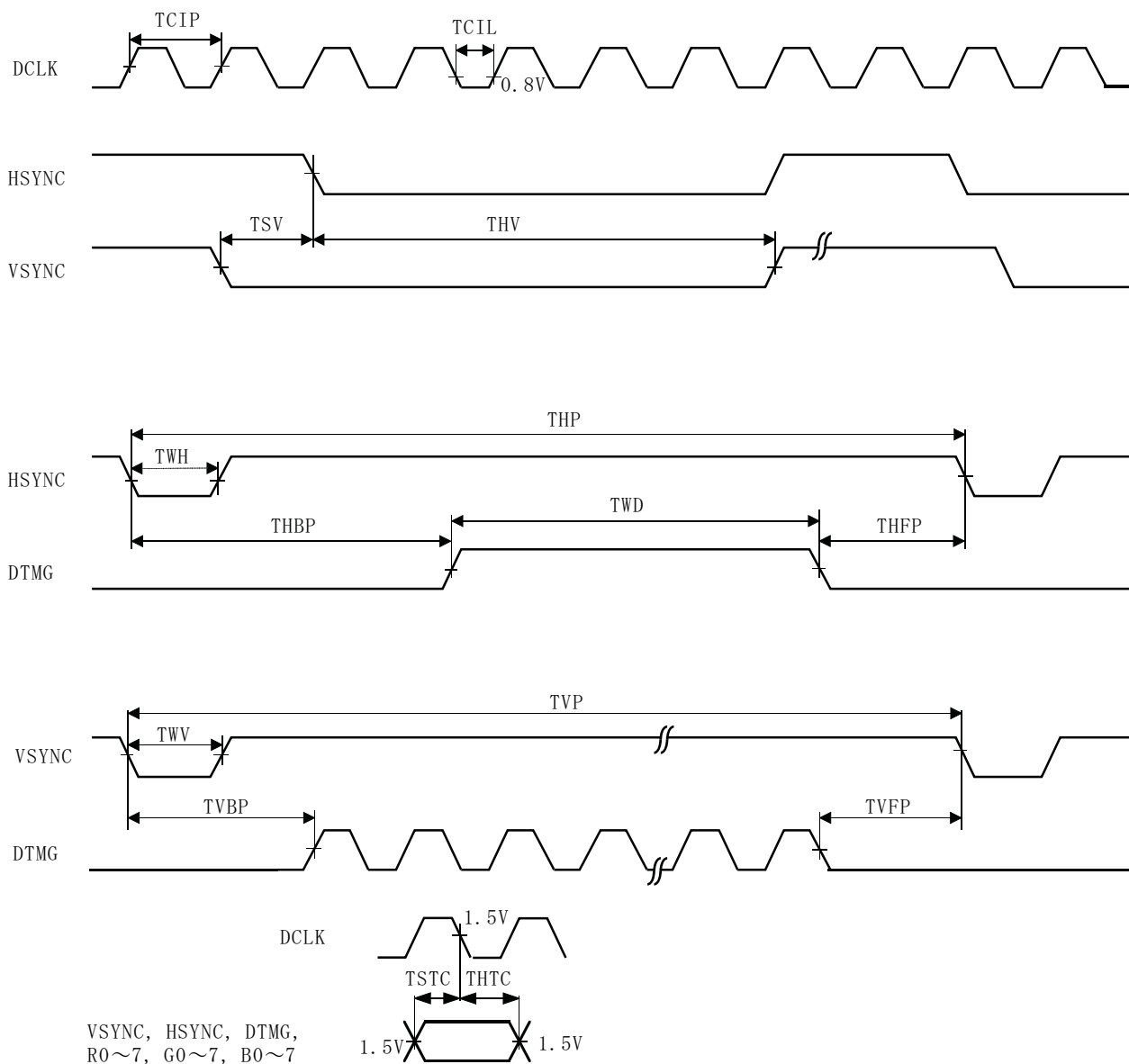
Notes 1) Definition of gray scale:

Color(n) . . . Number in parenthesis indicates gray scale level. Larger n corresponds to brighter level.

2) Data: 1:High, 0:Low

## 6. INTERFACE TIMING

### 6.1 TIMING CHART



- Notes
- 1) Reference level for each timing signal is 1.5V unless it is stated on the chart, high level voltage( $V_{IH}$ ) and low level voltage( $V_{IL}$ ) are defined as follows:  
 $V_{IH} \geq 2.0V$        $V_{IL} \leq 0.8V$   
 The above definition conforms to the specifications of LVDS transmitter (THC63LVDM83A / by THine Microsystems, Inc.).
  - 2) The timing of DCLK to other signals conforms to the specifications of LVDS transmitter.
  - 3) HSYNC, VSYNC timing is specified in negative polarity.
  - 4) HSYNC pulse is needed while data is invalid (blanking period).



## 6.2 INTERFACE TIMING SPECIFICATIONS

### 6.2.1 CTL=Low

Item		Symbol	Min.	Typ.	Max.	Unit	Note
DCLK	Frequency	fCLK	73.7	82	82.6	MHz	D=TCIL/TCIP
	Duty	D	0.35	0.5	0.65	—	
HSYNC	Frequency	fH	44.8	49.7	53.6	kHz	
	Period	THP	1646	1650	1708	TCIP	
	Width-Active	TWH	8	—	240	TCIP	
VSYNC	Frequency	fV	58	60	62	Hz	4)
	Set up Time	TSV	0	—	—	TCIP	to HSYNC
	Hold Time	THV	8	—	—	TCIP	
	Period	TVP	772	—	900	THP	
	Width-Active	TWV	1	—	120	THP	
DTMG	Horizontal Back porch	THBP	16	—	—	TCIP	
	Horizontal Front Porch	THFP	0	—	—	TCIP	
	Vertical Back Porch	TVBP	2	—	1)	THP	
	Vertical Front porch	TVFP	2	—	1)	THP	
	Width-Active	TWD	1280	1280	1280	TCIP	
COMMON	Set up Time	TSTC	5	—	2)	ns	
	Hold Time	THTC	3	—	2)	ns	

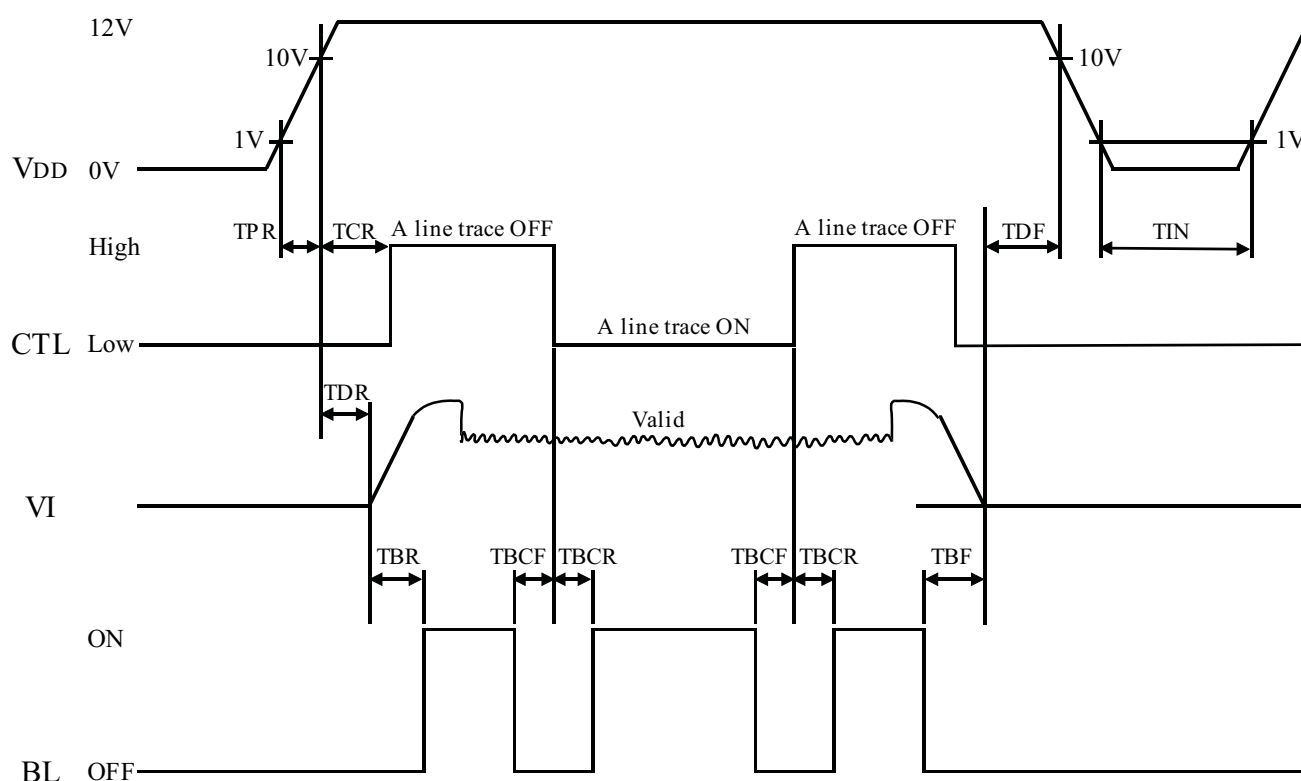
### 6.2.2 CTL=High

Item		Symbol	Min.	Typ.	Max.	Unit	Note
DCLK	Frequency	fCLK	73.7	82	82.6	MHz	D=TCIL/TCIP
	Duty	D	0.35	0.5	0.65	—	
HSYNC	Frequency	fH	41	49.7	53.6	kHz	
	Period	THP	1646	1650	2000	TCIP	
	Width-Active	TWH	8	—	240	TCIP	
VSYNC	Frequency	fV	48	60	62	Hz	4)
	Set up Time	TSV	0	—	—	TCIP	to HSYNC
	Hold Time	THV	8	—	—	TCIP	
	Period	TVP	772	—	900	THP	
	Width-Active	TWV	1	—	120	THP	
DTMG	Horizontal Back porch	THBP	16	—	—	TCIP	
	Horizontal Front Porch	THFP	0	—	—	TCIP	
	Vertical Back Porch	TVBP	2	—	1)	THP	
	Vertical Front porch	TVFP	2	—	1)	THP	
	Width-Active	TWD	1280	1280	1280	TCIP	
COMMON	Set up Time	TSTC	5	—	2)	ns	
	Hold Time	THTC	3	—	2)	ns	

In addition to the above, these timing should conforms to the followings.

- 1)  $TVBP+TVFP \geq 4 THP$
- 2) TSTC and THTC conforms to the specifications of LVDS transmitter.  
It is preferable to check the specifications of LVDS transmitter in your system.
- 3) TVP fluctuation should be kept within  $\pm 1$  line.
- 4) A line trace function does not allowed in PAL.

### 6.3 TIMING BETWEEN INTERFACE SIGNALS AND POWER SUPPLY



Timing of power supply voltage and input signals should be used under the following specifications.

$$0\text{ms} \leq \text{TPR} \leq 10\text{ms}$$

$$10\text{ms} \leq \text{TDR} \leq 50\text{ms}$$

$$0\text{ms} \leq \text{TDF} \leq 50\text{ms}$$

$$\text{TIN} \geq 1\text{s}$$

$$200\text{ms} \leq \text{TBR} \leq 500\text{ms}$$

$$\text{TBF} \leq 100\text{ms}$$

$$4\text{ms} \leq \text{TCR} \leq 10\text{ms}$$

$$0\text{ms} \leq \text{TBCF}$$

$$200\text{ms} \leq \text{TBCR}$$

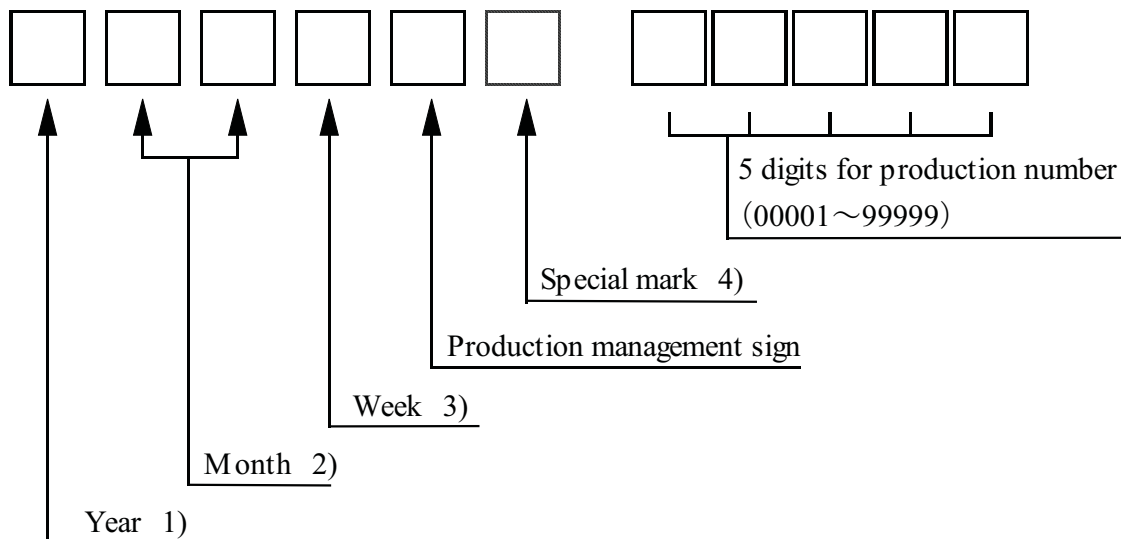
During CTL switching, follows timing should be kept.

- $1646 \leq \text{THP} \leq 2046$
- Don't continuously output timing  $\text{TVP} \leq 79$  or  $\text{TVP} \geq 2047$
- Don't change DCLK frequency.



## 8. DESIGNATION OF LOT MARK

### 8.1 LOT MARK



#### Notes

1)

Year	Mark
2003	3
2004	4
2005	5
2006	6

2)

Month	Mark	Month	Mark
1	01	7	07
2	02	8	08
3	03	9	09
4	04	10	10
5	05	11	11
6	06	12	12

3)

Week (Day)	Mark
1~7	1
8~14	2
15~21	3
22~28	4
29~31	5

- 4) It is the mark that was opened up by production person to take correspondence with production number.

### 8.2 Revision (REV.) control

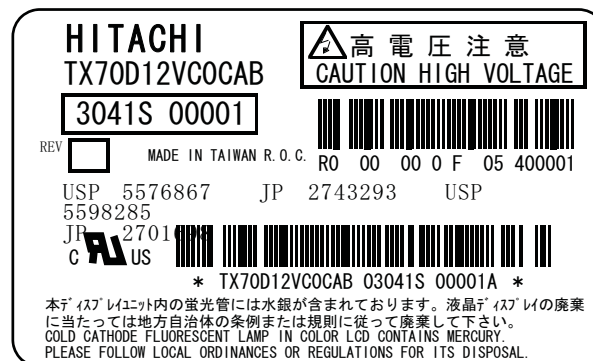
REV. is the column for manufacturing convenience. A-Z except I and O may be written on this column.

### 8.3 Location of lot mark

Lot mark is printed on a label. The label is on the metallic bezel as shown in 7. External Dimensional. The style of character will be changed without notice.



(a) Made in Japan



(b) Made in Taiwan R.O.C.

## 9. COSMETIC SPECIFICATIONS

### 9.1 Condition for cosmetic inspection

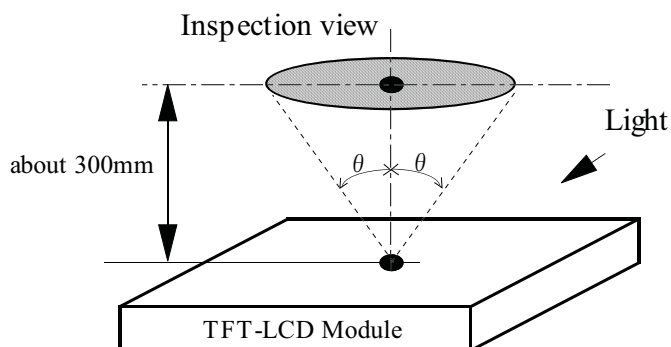
#### (1) Viewing zone

- a) The figure shows the correspondence between eyes (of inspector) and TFT-LCD module.

$\theta \leq 45^\circ$  : when non-operating inspection

$\theta \leq 5^\circ$  : when operating inspection

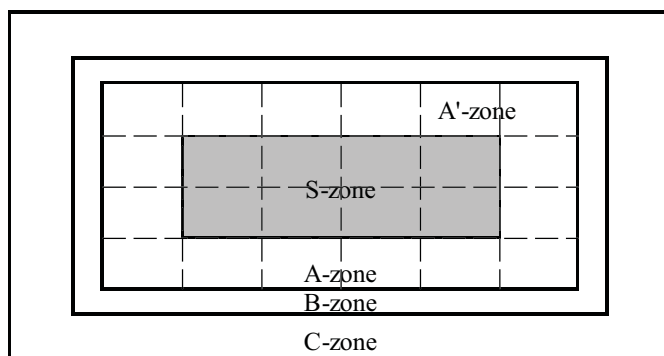
- b) Inspection should be executed only from front side and only A-zone.  
Cosmetic of B-zone and C-zone are ignore.  
(refer to 9.2 Definition of zone)



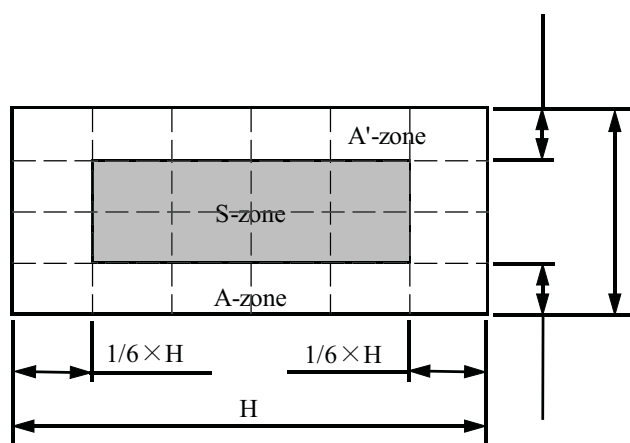
#### (2) Environmental

- a) Temperature : 25 degrees  
b) Ambient light : about 700 lx and non-directive when operating inspection.  
: about 1000 lx and non-directive when non-operating inspection.  
c) Back-light : when non-operating inspection, back-light should be off.

### 9.2 Definition of zone



- A-zone : Display area (pixel area)
- B-zone : Area between A-zone and C-zone
- C-zone : Metallic bezel area
- S-zone : Display center area
- A'-zone : Display area (A-zone except S-zone)





### 9.3 COSMETIC SPECIFICATIONS

When displaying conditions are not stable (ex. at turn on or off), the following specifications are not applied.

	No.	ITEM			Max. acceptable number		Unit	Note
					S-zone	A'-zone		
Operating inspection	1	Dot defect	Sparkle mode	1-dot	0		pcs	1),2),4)
				2-dots	0		Units	1),2),5)
				3-dots	0			
				4-dots	0			
				Density	0	pcs/ ϕ 20 <sub>mm</sub>	1),2),6)	
				Total	0	pcs	1),2)	
			Black mode	1-dot	7		pcs	1),3),4)
				2-dots	1		Units	1),3),5)
				3-dots	0			
				4-dots	0			
				Density	3	pcs/ ϕ 20 <sub>mm</sub>	1),3),6)	
				Total	7	pcs	1),3)	
			Total	7	pcs	1)		
	2	Line defect				Serious one is not allowed.	—	—
	3	Uneven brightness						
	4	Stain inclusion [ Line shape W : width(mm) L : length(mm) ]	W<=0.02	L : Ignore	Ignore		pcs	7)
			W<=0.04	L<=4.0	8			
				L>4.0	0			
			W<=0.08	L<=2.0	8			
				L>2.0	0			
			W>0.08	—	(See dot shape)			
	5	Stain inclusion [ Dot shape D : ave. dia.(mm) ]	D<=0.22		Ignore		pcs	7)
			D<=0.5		8			
			D>0.5		0			
	6	Scratch on polarizer [ Line shape W : width(mm) L : length(mm) ]	W<=0.02	L : Ignore	Ignore		pcs	8)
			W<=0.08	L<=20	10			
				L>20	0			
			W<=0.08	—	0			
	7	Scratch on polarizer [ Dot shape D : ave. dia.(mm) ]	D<=0.2		Ignore		pcs	8)
			D<=0.6		10			
			D>0.6		0			



	No.	ITEM		Max. acceptable number A-zone	Unit	Note
non-operating inspection	8	Bubbles, peeling in polarizer [ D : ave. dia.(mm) ]	D≤0.2	Ignore	pcs	8)
			D≤0.5	10		
			D>0.5	0		
	9	Wrinkles on polarizer		Serious one is not allowed.	-	-

Note 1) Dot defect : defect area > 1/2 dot

2) Sparkle mode : brightness of dot is more than 30% at black. (visible to eye)

3) Black mode : brightness of dot is less than 70% at white. (visible to eye)

4) 1 dot : defect dot is isolated, not attached to other defect dot.

5) N dots : N defect dots are consecutive. (N means the number of defects dots)

6) Density : number of defect dots inside 20mm  $\phi$ .

7) Those stains which can be wiped out easily are acceptable.

8) Polarizer area inside of B-zone is not applied.

9) No major (serious) defects when viewed in gray scale mode.

## 10. PRECAUTION

Please pay attention to the followings when a Super-TFT module with a back-light unit is used, handled and mounted.

### 10.1 Precaution to handling and mounting

- (1) Applying strong force to a part of the module may cause partial deformation of frame or mold, and cause damage to the display.
- (2) The module should gently and firmly be held by both hands. Never hold by just one hand in order to avoid any internal damage. Never drop or hit the module.
- (3) The module should be installed with mounting holes at each corner of a module.
- (4) Uneven force such as twisted stress should not be applied to a module when a module is mounted on the cover case. The cover case must have sufficient strength so that external force can not be transmitted directly to a module.
- (5) It is recommended to leave a space between a module and a holding board of a module so that partial force is not applied to a module.

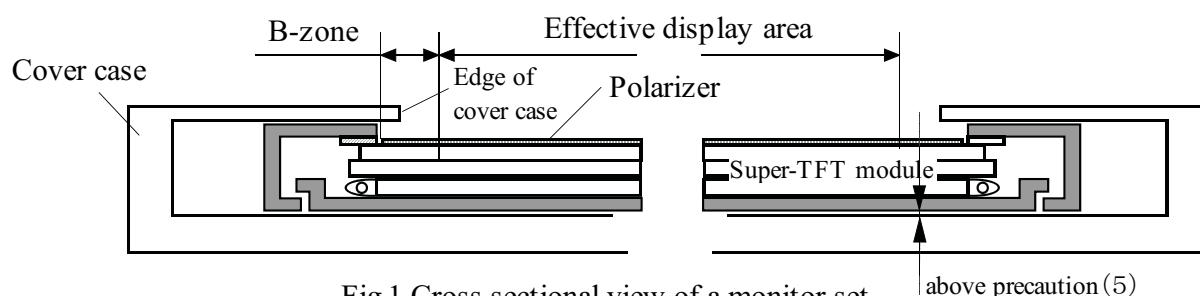


Fig.1 Cross sectional view of a monitor set

- (6) The edge of a cover case should be located inside more than 1mm from the edge of a module front frame.
- (7) A transparent protective plate should be added on the display area of a module in order to protect a polarizer and Super-TFT cell. The transparent protective plate should have sufficient strength so that the plate can not touch a module by external force.
- (8) Materials included acetic acid and choline should not be used for a cover case as well as other parts and boards near a module. Acetic acid attacks a polarizer. Choline attacks electric circuits due to electro-chemical reaction.
- (9) The polarizer on a TFT cell should carefully be handled due to its softness, and should not be touched, pushed or rubbed with glass, tweezers or anything harder than HB pencil lead. The surface of a polarizer should not be touched and rubbed with bare hand, greasy clothes or dusty clothes.
- (10) The surface of a polarizer should be gently wiped with absorbent cotton, chamois or other soft materials slightly contained petroleum benzene when the surface becomes dirty. Normal-hexane as cleaning chemicals is recommended in order to clean adhesives which fix front/rear polarizers on a Super-TFT cell. Other cleaning chemicals such as acetone, toluen and alcohol should not be used to clean adhesives because they cause chemical damage to a polarizer.
- (11) Saliva or water drops should be immediately wiped off. Otherwise, the portion of a polarizer may be deformed and its color may be faded.
- (12) The module should not be opened or modified. It may cause not to operate properly.

- (13) Metallic bezel of a module should not be handled with bare hand or dirty gloves. Otherwise, color of a metallic frame may become dirty during its storage. It is recommended to use clean soft gloves and clean finger stalls when a module is handled at incoming inspection process and production (assembly) process.
- (14) Lamp(CCFL) cables should not be pulled and held.

## **10.2 Precaution to operation**

- (1) The ambient temperature near the operated module should be satisfied with the absolute maximum ratings. Unless it meets the specifications, sufficient cooling system should be adopted to system.
- (2) The spike noise causes the mis-operation of a module. The level of spike noise should be as follows:  
-200mV<=over- and under- shoot of VDD<= +200mV  
VDD including over- and under- shoot should be satisfied with the absolute maximum ratings.
- (3) Optical response time, luminance and chromaticity depend on the temperature of a Super-TFT module. Response time and saturation time of CCFL luminance become longer at lower temperature operation.
- (4) Sudden temperature change may cause dew on and/or in the a module. Dew males damage to a polarizer and/or electrical contacting portion. Dew causes fading of displayed quality.
- (5) Fixed patterns displayed on a module for a long time may cause after-image. It will be recovered soon.
- (6) A module has high frequency circuits. Sufficient suppression to electromagnetic interference should be done by system manufacturers. Grounding and shielding methods may be effective to minimize the interference.
- (7) Noise may be heard when a back-light is operated. If necessary, sufficient suppression should be done by system manufacturers.
- (8) The module should not be connected or removed while a main system works.
- (9) Inserting or pulling I/F connectors causes any trouble when power supply and signal dates are on-state.I/F connectors should be inserted and pulled after power supply and signal dates are turned off.

## **10.3 Electrostatic discharge control**

- (1) Since a module consists of a Super-TFT cell and electronic circuits with CMOS-ICs, which are very weak to electrostatic discharge, persons who are handling a module should be grounded through adequate methods such as a list band. I/F connector pins should not be touched directly with bare hands.
- (2) Protection film for a polarizer on a module should be slowly peeled off so that the electrostatic charge can be minimized.

## **10.4 Precaution to strong light exposure**

- (1) A module should not be exposed under strong light. Otherwise, characteristics of a polarizer and color filter in a module may be degraded.

## **10.5 Precaution to storage**

When modules for replacement are stored for a long time, following precautions should be taken care of:

- (1) Modules should be stored in a dark place. It is prohibited to apply sunlight or fluorescent light during storage. Modules should be stored at 0 to 35°C at normal humidity (60%RH or less).
- (2) The surface of polarizers should not come in contact with any other object. It is recommended that modules should be stored in the Hitachi's shipping box.

## **10.6 Precaution to handling protection film**

- (1) The protection film for polarizers should be peeled off slowly and carefully by persons who are electrically grounded with adequate methods such as a list band. Besides, ionized air should be blown over during peeling action. Dusts on a polarizer should be blown off by an ionized nitrogen gun and so on.
- (2) The protection film should be peeling off without rubbing it to the polarizer. Because, if the film is rubbed together with the polarizer, since the film is attached to the polarizer with a small amount of adhesive, the adhesive may remain on a polarizer.
- (3) The module with protection film should be stored on the conditions explained in 10.5 (1). However, in case that the storage time is too long, adhesive may remain on a polarizer even after a protection film is peeled off. Besides, in case that a module is stored at higher temperature and/or higher humidity, adhesive may remain on a polarizer. The remained adhesive may cause non-uniformity of display image.
- (4) The adhesive can be removed easily with Normal-Hexane. The remained adhesive or its vestige on the polarizer should be wiped off with absorbent cotton or other soft materials such as chamois slightly contained Normal-Hexane.

## **10.7 Safety**

- (1) Since a Super-TFT cell and lamps are made of glass, handling to the broken module should be taken care sufficiently in order not to be injured. Hands touched liquid crystal from a broken cell should be washed sufficiently.
- (2) The CFL inverter should be designed to include the function of output shutdown in case the output overcurrent happen due to any backlight trouble.  
The shutdown function should be assured to work in abnormal condition at the actual system.
- (3) The module should not be taken apart during operation so that back-light drives by high voltage.

## **10.8 Environmental protection**

- (1) The Super-TFT module contains cold cathode fluorescent lamps. Please follow local ordinance or regulations for its disposal.
- (2) Flexible circuits board and printed circuits board used in a module contain small amount of lead. Please follow local ordinance or regulations for its disposal.

## **10.9 Use restrictions and limitations**

- (1) This product is not authorized for use in life support devices or systems, military applications or other applications which pose a significant risk of personal injury.
- (2) In no event shall Hitachi, Ltd., be liable for any incidental, indirect or consequential damages in connection with the installation or use of this product, even if informed of the possibility thereof in advance. These limitations apply to all causes of action in the aggregate, including without limitation breach of contract, breach of warranty, negligence, strict liability, misrepresentation and other torts.

## **10.10 Others**

- (1) Electrical components which may not affect electrical performance are subjective to change without notice because of their availability.

Hitachi Displays, Ltd.	Date	Apr.02,2009	Sheet No.	3284PS 2613 - TX70D12VC0CAB - 1	Page	13-3/3
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